REMARKS/ARGUMENTS

Favorable reconsideration of this application as currently amended and in view of the following discussion is respectfully requested.

Claims 1-4 are pending in the present application. Claim 4 is amended by the present amendment.

In the outstanding Office Action, the title was objected to; Claims 1-4 were rejected under 35 U.S.C. § 102(b) as anticipated by Shokouhi et al. (U.S. Patent No. 6,249,458, herein "Shokouhi"); and Claims 1-4 were rejected under 35 U.S.C. § 102(b) as anticipated by Shioyama (U.S. Patent No. 6,813,186).

Applicant thanks the Examiner for the courtesy of an interview extended to Applicant's representative on May 11, 2005. During the interview differences between the claims and the applied art were discussed. Further, clarifying claim amendments, similar to those presented herein, were also discussed. No agreement was reached, pending the Examiner's detailed consideration of the claim amendments upon formal submission. Arguments presented during the interview are reiterated below.

Initially, it is noted that the PTO-1449 form filed with an Information Disclosure Statement (IDS) on October 23, 2003, has been only partially acknowledged (the reference listed in the Foreign Patent Documents section has not been initialed as considered). Accordingly, it is respectfully requested that all references of the PTO-1449 form be initialed as considered. For the Examiner's convenience, a copy of the IDS and the accompanying documents is enclosed.

Regarding the objection to the title, the title has been amended to be more indicative of the claimed invention without adding new matter. Accordingly, it is respectfully requested this objection be withdrawn.

Regarding the rejection of Claims 1-4 under 35 U.S.C. § 102(b) as anticipated by Shokouhi, Claim 1 is maintained and Claim 4 is amended to clarify that a charge pump circuit and a port circuit are connected to a decoder through first and second switching circuits, respectively. The claim amendment finds support in Figure 4 and in its corresponding description in the specification. No new matter has been added.

Briefly recapitulating, independent Claim 1 is directed to a semiconductor memory that includes a plurality of bit lines, a Y decoder, and a disconnecting device provided between at least one of the plurality of bit lines and the Y decoder. The disconnecting device is configured to electrically disconnect the at least one of the plurality of bit lines and the Y decoder. In a non-limiting example, Figure 1 shows the plurality of bit lines 3 and 4, the Y decoder 1, and the disconnecting device 17 or 18.

As disclosed in the specification at page 7, line 23, to page 9, line 5, the semiconductor memory of Claim 1 advantageously distinguishes "an over-erased defective memory cell from a defect in the Y decoder."[1]

Turning to the applied art, Shokouhi shows in Figure 3 a semiconductor device having a bitline control circuit 800-B, a plurality of bit lines BL0-BLX, a decoder 850, and a switch 840. Further, the semiconductor device has another bitline control circuit 800-A that includes switches 820 and a transistor (unlabeled) connected through a line BLL to a switch BLL SWITCH 440. Shokouhi shows in Figure 8 a latch transistor 813 that is connected through the same line BLL to the switch BLL SWITCH 440, as the unlabeled transistor of Figure 3. Accordingly, it is respectfully submitted that the unlabeled transistor shown in Figure 3 is the latch transistor 813 of Figure 8 of Shokouki.

As discussed during the interview, the latch transistor 813 has a property to isolate (disconnect) a bitline, but the switch 840 of Figure 3 (identified by the outstanding Office

[1] Specification, page 7, lines 23-24.

Action as corresponding to the claimed disconnecting device) cannot disconnect the bitline. In this regard, Shokouhi specifically discloses at column 4, lines 61-66, that "[b]itline source switches **840** operate in a manner similar to bitline drain switches **830** ... to generates [sic] approximate voltage levels onto the bitlines BL**0** through BLX of memory array **125**." Thus, Shokouhi discloses a switch 840 that is not capable of switching off the bitline, but only supplying various voltages to the bitline.

Therefore, as discussed during the interview, Shokouhi does not teach or suggest a disconnecting device provided between at least one of the plurality of bit lines and the Y decoder, and configured to electrically disconnect the at least one of the plurality of bit lines and the Y decoder.

Accordingly, it is respectfully submitted that independent Claim 1 and each of the claims depending therefrom patentably distinguish over Shokouhi.

Regarding independent Claim 4, Claim 4 is directed to a semiconductor memory that includes, *inter alia*, a Y decoder, a charge pump circuit, and a port circuit. The charge pump circuit is connected to the Y decoder through a first switching circuit and the port circuit is connected to the Y decoder through a second switching circuit. Further, the port circuit is configured to supply an external voltage to the Y decoder.

In a non-limiting example, Figure 5 shows the Y decoder 1, the pump charge circuit 100, the port circuit 101, the first switching circuit 103, and the second switching circuit 104.

The outstanding Office Action asserts that Shokouhi shows in Figure 3 a charge pump circuit 810-B and a port circuit (the ISP circuit 300 shown in Figure 2), each being connected to the decoder 850 through a switching circuit. However, as discussed during the interview, Figure 3 shows that the decoder 850 is directly connected to the ISP circuit 300 with no switching circuit between the decoder 850 and the ISP circuit 300.

Accordingly, it is respectfully submitted that independent Claim 4 patentably distinguishes over Shokouhi.

Regarding the rejection of Claims 1-4 under 35 U.S.C. § 102(b) as anticipated by Shioyama, that rejection is respectfully traversed for the following reasons.

Shioyama shows in Figure 1 a memory device having a plurality of bit lines BL, a decoder YD, and a switching circuit P2. However, as discussed during the interview with regard to Claim 1, Shioyama does not teach or suggest a disconnecting device provided between at least one of the plurality of bit lines BL and the decoder, and configured to electrically disconnect the at least one of the plurality of bit lines and the decoder.

Accordingly, it is respectfully submitted that independent Claim 1 and each of the claims depending therefrom patentably distinguish over Shioyama.

Regarding Claim 4, the outstanding Office Action asserts at page 4, second full paragraph, that "the capacitance of the load applied to the switch circuits P2 and P4" corresponds to the claimed port circuit. However, Claim 4 has been amended to recite that the port circuit is configured to supply an external voltage to the Y decoder and, as discussed during the interview, Shioyama does not teach or suggest such port circuit. Applicant notes that a capacitance or a load is not a port circuit. In addition, Shioyama does not teach or suggest first and second switches for connecting the charge pump circuit and the port circuit to the decoder. It is also noted that switches P3 and P4 of Shioyama are not connected to the decoder YD (see Figure 1 of Shioyama).

Accordingly, it is respectfully submitted that independent Claim 4 patentably distinguishes over Shioyama.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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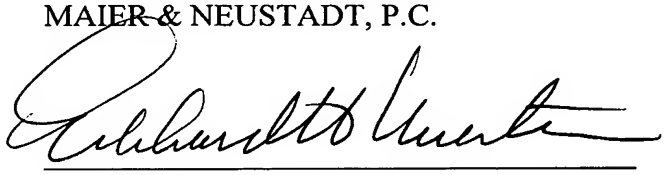

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